Listing of the Appealed Claims (All claims unless indicated as "canceled" are under Appeal)

1. (Canceled)

2. (Canceled) .

3. (Previously presented) The data serializer of claim 36, wherein said PLL locks to said signal from said FIFO to said phase detector.

4. (Previously presented) The data serializer of claim 36, wherein said wideband loop filter of said PLL comprises a wideband analog filter to suppress VCO phase noise and generate a low jitter clock.

5. (Previously presented) The data serializer of claim 36, wherein said narrow band loop filter of said DLL comprises a digital narrow band filter to filter noise from the data clock and set the jitter bandwidth..

6. (Previously presented) The data serializer of claim 36, wherein said signal representative of the fill rate of said FIFO register and inputted to said phase detector comprises a FIFO fill level indicator.

7. (Original) The data serializer of claim 6, wherein said phase detector is configured to translate said FIFO fill level into a digital value.

8. (Canceled)

9. (Previously presented) A dual loop retimer comprising the data serializer of claim 36.

10. (Currently amended) In a plesiochronous system, a method for PLL/DLL data serialization comprising:

detecting a local reference at a phase/frequency detector (PFD) of a phase lock loop (PLL);

phase locking a voltage controlled oscillator (VCO) of said PLL to a local reference to suppress a phase noise of said VCO;

receiving a parallel data input and a data clock at a FIFO register;

filtering, at a delayed lock loop (DLL), a signal representative of a fill level of said FIFO;

phase shifting an output of said VCO of said PLL in response to said filtering step;

locking said PLL to a frequency corresponding to a pre-filtered signal input to said DLL;

receiving, at a parallel-in serial-out (PISO) serializer, said parallel data and said VCO output; and

outputting a serialized data from said PISO serializer with said VCO ~~output~~ outputting a transmit clock.

11. (Original) The method of claim 10, further comprising the step of outputting a synthesized clock.

12. (Original) The method of claim 10, wherein said PLL filtering step comprises wide bandwidth filtering.

13. (Original) The method of claim 10, wherein said DLL filtering step comprises narrow bandwidth filtering.

14. (Original) The method of claim 10, further comprising the step of translating said signal in said DLL to a digital value.

15. (Original) The method of claim 14, wherein said translating step comprises a phase detector in said DLL.

16. (Canceled)

17. (Currently amended) A plesiochronous data retimer comprising:

a digital delay lock loop (DDLL) receiving an input data to be retimed and configured to recover a clock of said input data;

a phase/frequency detector (PFD) receiving a local reference;

a phase shifter configured in a feedback loop with said PFD;

a first loop filter coupled to said phase shifter;

said phase/frequency detector (PFD), phase shifter and first loop filter forming a ~~dual loop serializer~~ phase locked loop,

a serial-in and parallel-out (SIPO) ~~(serial-in and parallel-out)~~ deserializer coupled to said input data;

a first-in first-out FIFO register coupled to said deserializer ~~and said dual loop serializer DLL~~; and

a parallel-in serial-out (PISO) ~~(parallel-in and serial-out)~~ serializer receiving said deserialized input data and transmitting a serialized data.

18. (Original) The retimer of claim 17, wherein said DDLL comprises a phase detector and a digital loop filter.

19. (Original) The retimer of claim 18, wherein said DDLL comprises a wide bandwidth.

20. (Currently amended) The retimer of claim 18, ~~wherein said serializer~~ further comprising a second ~~comprises a~~ loop filter ~~within said PLL~~.

21. (Currently amended) The retimer of claim 20, further comprising ~~wherein said serializer comprises~~ a dual bandwidth.

22. (Canceled)

23. (Previously presented) A plesiochronous data retiming method comprising:

recovering a clock from a received serial input data at a digital delay locked loop (DDLL);

deserializing said serial data to a parallel data using said recovered clock;

writing said parallel data to a FIFO (first-in first-out);

synthesizing a transmit clock;

reading said parallel data from said FIFO;

serializing said parallel data using said synthesized transmit clock;

detecting a FIFO fill level at a delay locked loop (DLL); and

phase shifting, in a phase lock loop (PLL), an output of a VCO, wherein said phase shifting is in response to said detecting step.

24. (Original) The retiming method of claim 23, wherein said synthesizing step comprises phase locking said VCO to a local reference.

25. (Original) The retiming method of claim 23, further comprising translating said FIFO fill level to an integrating value.

26. (Original) The retiming method of claim 23, wherein said writing step and said reading step comprise a write clock of said FIFO and a read clock of said FIFO, respectively.

27. (Original) The retiming method of claim 26, further comprising phase locking said write and read clocks of said FIFO in said DLL.

28. (Original) The retiming method of claim 26, further comprising locking said VCO output to said FIFO write clock.

29. (Original) A method for PLL/DLL data retiming comprising:

recovering a clock from a received serial input data at a digital delay locked loop (DDLL);

writing said serial data to a FIFO (first-in first-out);

synthesizing a transmit clock;

reading a retimed data from said FIFO;

detecting a FIFO fill level at a delay locked loop (DLL); and

phase shifting, in a phase lock loop (PLL), an output of a VCO, wherein said phase shifting is in response to said detecting step.

30. (Original) The method of claim 29, further comprising the step of outputting a synthesized clock.

31. (Original) The method of claim 29, further comprising the step of phase locking said VCO of said PLL to a local reference to suppress a phase noise of said VCO.

32. (Original) The method of claim 31, wherein said PLL filtering step comprises wide bandwidth filtering.

33. (Original) The method of claim 29, further comprising the step of translating said FIFO fill level to an integrating value.

34. (Original) The method of claim 33, wherein said translating step comprises a phase detector in said DLL.

35. (Original) The method of claim 29 comprising a plesiochronous system.

36. (Currently amended) In a plesiochronous system, a dual loop data serializer comprising:

a first-in-first-out (FIFO) register, having a fill rate, and receiving a parallel data input and a data clock input and providing a plurality of outputs;

a parallel-in serial-out (PISO) serializer having an input coupled to one of the plurality of outputs of said FIFO register, for receiving an input signal from said FIFO register, and outputting serialized data;

a phase detector, having ~~an~~ at least one input coupled to at least one of the plurality of outputs ~~an output~~ of said FIFO register, for receiving a signal representative of the fill rate of said FIFO register, said phase detector having an output for providing an output signal;

a narrow band loop filter coupled between said output of said phase detector and a phase

shifter ~~having an input coupled to the output of said phase detector~~ and configured to provide an output to a phase shifter, thereby producing a phase shift in a PLL;

~~a~~ the phase shifter having a first input ~~coupled to~~ adapted to receive the output signal from ~~of~~ said narrow band loop filter and providing an output signal to a phase/frequency detector;;

~~a~~ the phase/frequency detector having an input for receiving the output signal from ~~of~~ said phase shifter and also receiving a local reference input, and providing an output signal to a wideband loop filter;

~~a~~ the wideband loop filter having an input for receiving the output signal from the phase/frequency detector ~~coupled to the output of the phase/frequency detector~~ to suppress phase noise and adapted to provide ~~providing~~ an output signal to a voltage controlled oscillator (VCO);

a the voltage controlled oscillator (VCO) having an input adapted to receive ~~coupled to~~ the output signal from ~~of~~ said wideband loop filter, and adapted to provide ~~providing~~ a synthesized clock output signal to said PISO serializer and also to a second input of said phase shifter;

said phase shifter, phase/frequency detector, and wideband loop filter forming a phase locked loop with the VCO, such that the phase and frequency of the synthesized clock output signal of the VCO is modified by the output signal from ~~of~~ the narrow band loop filter; and

said PISO serializer providing the synthesized clock signal to said FIFO register;

whereby said phase detector compares the ~~received~~ data clock with the synthesized clock signal.

37. (New) In a plesiochronous system, a dual loop data serializer, as in claim 36, and further comprising:

a digital delay lock loop (DDLL) receiving an input data signal to be retimed and configured to recover a clock of said input data signal, said DDLL providing an output to a decision circuit;

the decision circuit receiving the output of said DDLL and also receiving said input data signal; and

a serial-in and parallel-out (SIPO) deserializer coupled between said decision circuit and said first-in first-out (FIFO) register for providing a parallel data input to said first-in first-out (FIFO) register.